## REMARKS

Claims 1-21 are pending in the current application. Of those, claims 1, 7, 10, and 20 are independent claims. Claims 1, 7, 10, and 20 are amended by this Response. No claims are canceled by this Response. New claim 21 is added by this Response.

## Discussion of Example Embodiments

Example embodiments may be directed to checking the operating speed of a processor after an operating mode or frequency has already been entered and using either the high speed control circuit or the low speed control circuit to control operations of periphery devices and/or a processor core. Accordingly, in example embodiments the processor (e.g., the high speed control circuit and low speed control circuit) may already be operating at a certain mode/frequency in order for the determination to be made because the determination may be made based on the operating state or frequency of the high and low speed control circuits. However, in Amos the determination of which multiplexer input to use may be made before the processor is operating at said multiplexer input. In particular, Amos waits until the high frequency oscillator 108 is powered up before actually switching an output of the multiplexer 106 to the input received from the high frequency oscillator 108.

## Claim Rejection – 35 U.S.C. § 112

Claims 1-5 and 7-20 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Applicant respectfully traverses this rejection.

The Examiner cites paragraphs [0025] and [0036] as being contradictory about the proper definition of the term "processor." Applicant respectfully submits that these paragraphs are not contradictory. In particular, paragraph [0025] discusses a processor 200. Paragraph [0036]

discusses a processor core 260. As disclosed at paragraph [0024] the processor 200 may include the processor core 260. Therefore, it is not contradictory to say that the processor 200 may be used with, hand-held devices such as a mobile telephone and a personal digital assistant (PDA), or in other devices, while at the same time saying that the processor core 260 may be used in these devices as disclosed at paragraphs [0025] and [0036]. Applicant respectfully submits that the processor 200 is clearly defined in the specification such that it may be interpreted as a "processor system" for at least the reason that paragraph [0024] and FIG. 2 clearly define that the processor 200 may include a control circuit 210, a multiplexer 250, a processor core 260, and/or a peripheral device. Accordingly, one skilled in the art would readily recognize that the processor 200 may include more features that the Examiner's more traditional interpretation of a processor. For example, the specification also contrasts the processor 200 to the processor core 260 included in the processor 200. In particular, Applicant respectfully submits that Applicant may call element 200, which includes the processor core 260, the control circuit 210, etc., whatever Applicant chooses, and in the present application Applicant chooses to call element 200 a processor. Therefore, element 200, i.e., the processor 200, is clearly enabled by the detailed description thereof in the specification which describes the processor 200 as including, among other elements, the processor core 260.

In view of the above, Applicant respectfully requests the rejections under 35 U.S.C. § 112 be withdrawn.

**Claim Rejections – 35 U.S.C. § 102**

Claims 1-20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Amos (US 6,934,870, hereinafter "Amos"). Applicant respectfully traverses this rejection.

Amos discloses at FIG. 1 a MAC 102 receiving its clocking signal from a clock multiplexer 106. A clock select line 107 from the MAC 102 is used to select one of the inputs to the multiplexer 106. The clock multiplexer 106 has a first input from a high frequency oscillator 108, a second input from a low frequency oscillator 110, and a third input from a PCI interface. An enable line 120 connecting the MAC 102 to the high frequency oscillator 108 allows the MAC to power on and power off the high frequency oscillator, and an enable line similar to 120 may also be connected to the low frequency oscillator 110 in order to power it on and off.

Amos further discloses at col. 4, lines 53-58 "The present invention may be used in cooperation with these different power states. This is especially true if the system has the enabled ability to receive a wakeup event back to the host system for the generation of PME# events or STSCHG# events which are used to wake up the host system."

Amos also discloses at col. 5, lines 45-53 with regard to FIG. 3 "If at step 308 the MAC 102 determines that it must operate in an active mode, then the MAC 102 sends a signal on enable line 120 to activate the high frequency oscillator 108 as shown in step 318. This can occur when the bus delivers a packet for transmission. As shown in step 320, the MAC 102 waits until the high frequency oscillator 108 is fully activated, typically 20 ms. At step 324 the MAC 102 sends a signal on the clock select line 107 to the clock multiplexer to switch to the high frequency oscillator 108."

Amos does not disclose outputting a selection signal based specifically on a determination of operating states or frequencies of a high-speed and low-speed control circuit. To the contrary, as noted above, Amos merely generally describes that the MAC 102 determines that it must operate in active mode and that different power states may be used. Amos does not disclose that this determination is made based on operating states or frequencies of its high frequency oscillator 108 or its low frequency oscillator 110.

Although Amos does disclose that the MAC 102 waits until the high frequency oscillator 108 is fully activated before sending a signal on the clock select line 107 to the clock multiplexer to switch to the high frequency oscillator 108, there is no indication in Amos that this waiting period is determined based on an operating state or frequency of the oscillator. To the contrary, FIG. 1 of Amos clearly shows that the MAC 102 does not receive any signals from the high frequency oscillator 108 besides the indirect clocking signal from the multiplexer 106, let alone a signal indicating an operating state or frequency of the high frequency oscillator 108.

As noted above in the discussion of example embodiments, in Amos the determination of which multiplexer input to use may be made before the processor is operating at said multiplexer input. In particular, Amos waits until the high frequency oscillator 108 is powered up before actually switching an output of the multiplexer 106 to the input received from the high frequency oscillator 108. Therefore, Amos fails to disclose "a selecting circuit for determining at least one of operation states and operating frequencies of a high-speed control circuit and a low-speed and low-power control circuit **based on direct monitoring of the high-speed control circuit and the low-speed and low-power control circuit** and for outputting a selection signal based on the determination" as required by claim 1. Claims 7, 10, and 20 contain features somewhat similar to those discussed above in regard to claim 1, and therefore, claims 7, 10, and 20 are patentable for at least somewhat similar reasons as claim 1. Claims 2-6, 8-9, and 11-19, which depend from one of claims 1, 7, 10, and 20, are patentable for at least the same reasons discussed above in regard to claims 1, 7, 10, and 20 as well as on their own merits.

In view of the above, Applicant respectfully requests the rejections under 35 U.S.C. § 102(e) be withdrawn.

## New Claim

New claim 21, which depends from claim 1, is patentable for at least the same reasons discussed above in regard to claim 1 as well as on its own merits.

## CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of the claims in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____

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